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20-4652P

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IN THE U.S. PATENT AND TRADEMARK OFFICE

Applicant:	Narihiro MOROSAWA et al.		
Application No.:	09/471,173	Group:	2826
Filed:	December 23, 1999	Examiner:	M. Brian
For:	INSULATED GATE TRANSISTOR AND PROCESSOR FABRICATING THE SAME		

REPLY TO RESTRICTION REQUIREMENT

Assistant Commissioner for Patents
Washington, DC 20231

February 23, 2001

Sir:

In reply to the Restriction Requirement dated January 23, 2001, the following remarks are respectfully submitted in connection with the above-identified application.

REMARKS

Claims 1-12 remain in connection with the present application.

The Examiner has restricted Applicants to election of one of the following inventions as follows:

Group I, claims 1-6, allegedly drawn to an insulated gate transistor; or

Group II, claims 7-10, allegedly drawn to a process of making an insulated gate transistor.

In response to the Examiner's request, Applicants hereby elect, ~~the~~ invention of Group I, claims 1-6 for prosecution in connection with the present application. An early indication of the allowability of each of claims 1-6 in connection with the present application is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Donald J. Daley, Reg. No. 34,313.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By _____
Donald J. Daley, Reg. No. 34,313

DJD:kna

P.O. Box 747
Falls Church, VA 22040-0747
(703) 205-8000